REMARKS

This is in response to the non-final Official Action currently outstanding with regard to the above-identified application.

Claims 1-24 were pending in this application at the time of the issuance of the currently outstanding Official Action. By the foregoing Amendment, Claims 1, 2, 3, 5, 9, 10, 11,13, 15, 19 and 22 have been amended to more clearly and distinctly state the subject matter that Applicants regard as their invention. No claims have been cancelled, added or withdrawn. Accordingly, upon the entry to the foregoing Amendment, Claims 1-7 and 9-24 as hereinabove amended will constitute the claims pending in this application.

The claims as they will stand upon the entry of the foregoing amendment are reproduced above as required by the Rules.

In the currently outstanding Official Action, the Examiner has:

1. Failed to re-acknowledged Applicants claim for foreign priority under 35 USC 119(a)-(d) or (f), and reconfirm the receipt of the required copies of the priority documents for this application by the United States Patent and Trademark Office – **Appropriate re-acknowledgment and reconfirmation in response to this communication is respectfully requested for the sake of good order and clarity of the record**;

2. Provided Applicants with a copy of the Form PTO/SB/08a/b that accompanied their Information Disclosure Statement of 28 January 2005 duly signed, dated and initialed by the Examiner in confirmation of his consideration of the art listed therein;

3. Failed to reconfirm that the drawings filed as on 20 May 2004 are accepted – **Appropriate reconfirmation of the acceptability of the drawings in response to this communication is respectfully requested**;

4. Provided Applicants with a Notice of References Cited (Form PTO-892);

5. Rejected Claims 1-7, 9 and 11-21 under 35 USC 102(b) as being unpatentable over Japanese Publication 10326084 to Goto Hisashi; and

6. Indicated that Claims 10 and 22-24 are allowed;

7. Indicated that the Fujita reference (US Patent 6,107,981) is cited as being pertinent to Applicants' disclosure, but is not relied upon in the rejection of any of the pending claims.

With respect to items 1-4, 6 and 7, Applicants respectfully submit that no further comment in these Remarks is required.

As was the case previously in this prosecution, Applicants' response to the currently outstanding substantive rejections of the claims of the above-identified application is that the reference upon which the Examiner relies does not support the Examiner's characterization of it when that reference is fully considered and understood.

In this regard, Applicants have previously pointed out that the present invention has the objectives of reducing power consumption in a signal line drive circuit without adverse impact upon the operating characteristics thereof; providing an image display device that utilizes that signal line drive circuit; and providing portable apparatus utilizing that signal line drive circuit. Further, Applicants have noted that to accomplish these objectives the present invention (i) eliminates an unnecessary circuit from prior art configurations, (ii) eliminates the current that would otherwise be used in the eliminated circuit, and (iii) avoids the occurrence of charging/discharging stray capacitance between bus lines when the image signal represents a small number of tones.

With reference to item 5 above, it is noted that the Examiner now has rejected Claims 1-7, 9 and 11-21 under 35 USC 102(b) as being anticipated by Japanese Publication 10326084 to Goto Hisashi (hereinafter "Hisashi"). Specifically, the Examiner consistently throughout the currently outstanding Official Action indicates a belief that in the Hisashi reference two first reference voltages (VDD2 and ground) are ***directly transmitted*** to the voltage chooser circuit as voltages Vo and V15. Applicants respectfully disagree and request reconsideration.

Accordingly, Applicants respectfully submit that an important technical difference between the present invention and the Hisashi reference lies in ***whether or not multiple first reference voltages from external first reference voltage supply means are provided directly to the reference voltage chooser circuit.***

More specifically, Applicant respectfully submits that in the present invention multiple first reference voltages are provided ***directly*** to the voltage chooser circuit from external first reference voltage supply means, but that in the Hisashi reference this is not the case. The reason for this lies in the difference between the techniques utilized by Hisashi and the present invention in the determination of which image tones are to be displayed (i.e., functional considerations not directly pertinent to the differences in structure between the present claims and the cited art) and in the ability of the present invention to avoid deterioration of the image to be displayed.

Accordingly, in the signal line drive circuit and image display device according to the present invention, the reference voltage chooser circuit receives not only (i) the second reference voltage obtained by dividing the first reference voltages, but also (ii) ***multiple*** first reference voltages **directly from** the external first reference voltage supply means. In other words, the reference voltage chooser circuit of the present invention receives two different types of reference voltages in two different ways. The multiple first reference voltages are provided directly from the external first reference voltage supply means to the voltage chooser circuit, and the second reference voltages created by voltage division from the first reference voltages are provided to the reference chooser circuit via buffers.

In Hisashi, on the other hand, no first reference voltage is provided **directly** to the voltage chooser circuit. Instead, ***a single*** first reference voltage VDD2 is provided to the voltage chooser circuit via a buffer as the voltage Vo and second reference voltages V1-V15 created by voltage division between VDD2 and ground also are provided to the voltage chooser circuit via buffers (i.e., the structure of the Hisashi reference includes buffers that respectively correspond to ***all*** of the tones of the sampled image, see, Hisashi at Claim 1, lines 3-4).

Applicants respectfully note in the latter regard that contrary to the Examiner's assertion in the currently outstanding Official Action, the voltage V15 ***is not*** ground, but rather is some portion of VDD2 determined by the ratio of the resistor located between the input to the buffer associated with SW15 and ground on the one hand, and the remainder of the resistors in the voltage division circuit shown in the Hisashi reference (see particularly, Fig. 3) on the other hand.

Hence. Applicants respectfully submit that the Hisashi reference fails to teach, disclose or suggest ***multiple*** first reference voltages provided ***directly*** to the voltage chooser circuit. In other words, even if one assumes a total pass though by the Hisashi buffers when the switches associated with the buffers are activated by VSYNC (12), the Hisashi reference is respectfully submitted to teach, disclose or suggest ***only a single first reference voltage from an external reference voltage supply means provided to the voltage chooser circuit via the buffer associated with SW0 in Hisashi's Fig. 3***. Accordingly, Applicants respectfully submit that the Hisashi reference fails to teach, disclose or suggest all of the limitations of the present claims such that it fails as an anticipatory reference under 35 USC 102(b). A decision so holding in response to this communication is respectfully requested.

In the above regards, it will be understood that according to the present invention, the first reference voltages supplied continuously to the voltage chooser circuit portion of the signal line drive circuit prevent the deterioration of display quality even when the first switch is OFF such that no power voltage is supplied to all of the buffers. This allows a reduction in the current consumption (power consumption) in the buffers. (See, page 17, lines 12-24, and Fig. 1 of the present specification).

In the Hisashi device, on the other hand, the voltage chooser circuit receives input voltage only while the switch is ON. When the switch is OFF, the application of voltage, including the constant voltage VDD2, to the buffers is cut off with the result that the buffers stop operating and substantially no bias current flows therethrough. (See, Hisashi at paragraph 0009, lines 28-31) Accordingly, when the current consumption (power consumption) in the buffers is reduced in the Hisashi reference by turning the switch OFF, there is an inevitable deterioration in the quality of the display unlike the situation with respect to the present invention.

Further, with specific regard to Claims 7 and 17, Applicants respectfully note that by adopting the structures herein claimed the number of bus lines to which the image signal is supplied can be reduced. This also allows for the reduction of the power required by the device (i.e., reduces power consumption) according to the number of tones required for the transmission of the data via the bus lines.

As stated previously in this prosecution, a main feature of Claim 7 is that ***a decoder circuit*** controlling the reference voltage chooser circuit ***is controlled through a third control signal to change a decoder table determined by the number of tones represented by a sampling signal generated by a sampling of the image signal***, whereby the reference voltage chooser circuit changes a reference voltage choosing pattern of the signal line driving circuit. Claim 17 incorporates these features into the display device therein claimed. In either case, however, it will be understood that the decoder table can be changed in accordance with the number of tones represented by the image signal. Consequently, the signals transmitted by the bus lines are fixed when the image signal represents a small number of tones. This fixation prevents the occurrence of the charging/discharging of stray capacitances between the bus lines thereby also reducing the power consumption of the signal line driving circuit.

More particularly, conventionally in cases where for example 6 bus lines are provided (i.e., a 6 bit mode), signals indicative of "1" and "0" need to be supplied to all six bus lines so as to express "white" or "black". In cases wherein 6 bus lines are provided in the context of the present invention as claimed in Claims 7 and 17, however, a signal indicative of "1" or "0" has to be supplied to only one bus line so as to express "white" or "black" while the signals supplied to the other bus lines can remain fixed to "0" or "1". The Hisashi reference, on the other hand, does not teach, disclose or suggest a structure for "reducing the number of bus lines to which the image signal is supplied or a structure for reducing power consumption equivalent to that presently claimed in Claims 7 and 17.

Therefore, it will be understood that a main feature of the present invention is that the claimed structure includes reference voltage means ***directly*** inputting (i.e., directly transmitting without the intervention of other circuit elements) ***multiple*** first reference voltages supplied by external first reference voltage supply means to a reference voltage chooser circuit. With that arrangement, no buffer circuit is required for the reference voltage line(s) directly transmitting the first reference voltages. Therefore, the signal line drive circuit takes up a smaller area and eliminates the amount of current that would otherwise be utilized by buffer circuits associated respectively with the first reference voltages. This results in power savings by the claimed signal line drive circuit in comparison to the prior art.

Hence, Applicants respectfully submit that since the Hisashi reference discloses at best the application to the voltage chooser circuit of only a single (not multiple) first reference voltage from an external reference voltage source via a buffer (not directly), the Hisashi reference cannot anticipate the present invention as herein claimed under 35 USC 102 either from a structural point of view or from the functional/contextual considerations argued previously and mentioned above.

The law is clear that "a claim is anticipated only if each and every element ***as set forth in the claim*** is found either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Company of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) The ***identical invention*** must be shown in as complete detail as contained in the...claim. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989) The elements must be arranged as required by the claim... *In re Bond,* 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990) *Emphasis added.*

As discussed in detail above, the cited references do not satisfy these standards because none of those references disclose all of the components (claimed features/limitations) of the present invention functioning in the same way relative to one another as herein claimed.

For each and all of the foregoing reasons, Applicants respectfully submit that that the reference currently relied upon by the Examiner when fully considered as to its true content does not support the Examiner's characterizations of it. In addition, Applicants respectfully submit that the reference relied upon by the Examiner is insufficient to establish a *prima facie* case supporting the Examiner's assertion that the claims of this application as hereinabove amended are not patentable.

Consequently, in view of the foregoing Amendment and Remarks, Applicants respectfully submit that the claims of this application as hereinabove amended are in condition for allowance. Therefore, entry of the foregoing Amendment, reconsideration, and allowance of the claims of this application as set forth hereinabove in response to this communication are respectfully requested.

Finally, Applicants believe that additional fees are not required for consideration of the foregoing Amendment After Final Rejection Under 37 CFR 1.116. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105** therefor.

Respectfully submitted,

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